16 V, 4 MHz Rail-to-Rail Output Amplifiers

AD8665/AD8666/AD8668

FEATURES

Offset voltage: 2.5 mV max
Low input bias current: 1 pA max
Single-supply operation: 5 V to 16 V
Dual-supply operation: ±2.5 V to ±8 V
Low noise: 8 nV/√Hz @ 10 kHz
Wide bandwidth: 4 MHz
Rail-to-rail output
Unity-gain stable
Lead-free packaging

APPLICATIONS

Sensor amplification
Reference buffers
Medical equipment
Physiological measurements
Signal filters and conditioning
Consumer audio
Photodiode amplification
ADC driver
Level shifting circuits

GENERAL DESCRIPTION

The AD866x family are single supply, rail-to-rail output amplifiers with low noise performance featuring an extended operating range with supply voltages up to 16 V. They also feature low input bias currents, wide signal bandwidth, and low input voltage and current noise. For lower offset voltage, choose the AD8661/AD8662/AD8664 family.

The combination of low offsets, very low input bias currents, and wide supply range make these amplifiers useful in a wide variety of cost sensitive applications normally associated with much higher priced JFET amplifiers. Systems using high impedance sensors, such as photo diodes, benefit from the combination of low input bias current, low noise, and low offset and bandwidth. The wide operating voltage range matches high performance ADCs and DACs. Audio applications and medical monitoring equipment can take advantage of the high input impedance, low voltage and current noise, wide bandwidth, and the lack of popcorn noise found in many other low input bias current amplifiers.

The AD866x family is specified over the extended industrial temperature range (−40°C to +125°C).

PIN CONFIGURATIONS

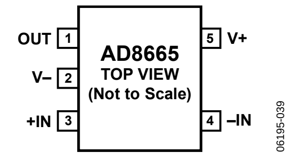

Figure 1. AD8665, 5-Lead SOT-23 (RJ-5)

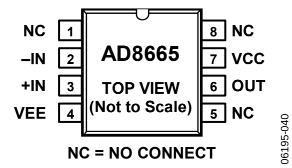

Figure 2. AD8665, 8-Lead SOIC_N (R-8)

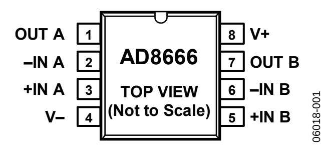

Figure 3. AD8666, 8-Lead SOIC_N (R-8)

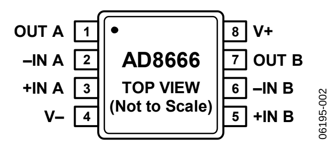

Figure 4. AD8666, 8-Lead MSOP (RM-8)

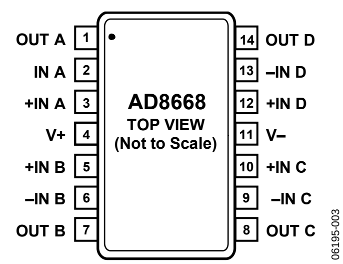

Figure 5. AD8668, 14-Lead TSSOP (RU-14)

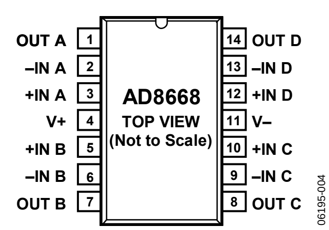

Figure 6. AD8668, 14-Lead SOIC_N (R-14)

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

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REVISION HISTORY

10/06—Rev. 0 to Rev. A

Added AD8665 .... Universal
Added New Figure 1 and Figure 2,
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Changes to Ordering Guide 13

4/06—Rev 0: Initial Version

SPECIFICATIONS

V_{DD} = 5.0 V, V_{CM} = V_{DD}/2, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	V_{CM} = 2.5 V		0.7	2.5	mV
		V_{CM} = −0.1 V to +3.0 V			3.0	mV
		−40°C < T_A < +125°C			5.0	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C < T_A < +125°C		3.0	10	μV/°C
Input Bias Current	I_B			0.2	1	pA
		−40°C < T_A < +125°C			550	pA
Input Offset Current	I_{OS}			0.1	0.5	pA
		−40°C < T_A < +125°C			70	pA
Input Voltage Range	V_{CM}		−0.1		+3.0	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = −0.1 V to +3.0 V	84	100		dB
		−40°C < T_A < +125°C	79			dB
Large-Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, V_O = 0.5 V to 4.5 V	68	145		V/mV
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_{OUT} = 1 mA	4.88	4.93		V
		−40°C < T_A < +125°C	4.86			V
Output Voltage Low	V_{OL}	I_{OUT} = 1 mA		50	85	mV
		−40°C < T_A < +125°C			105	mV
Short-Circuit Output Current	I_{SC}			±19		mA
Closed-Loop Output Impedance	Z_{OUT}	At 1 MHz, A_V = 1		50		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{DD} = 5.0 V to 16 V	98	115		dB
		−40°C < T_A < +125°C	94			dB
Supply Current per Amplifier	I_{SY}			1.1	1.4	mA
		−40°C < T_A < +125°C			2.0	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ		3.5		V/μs
Gain Bandwidth Product	GBP			4		MHz
Phase Margin	Φ_M			70		Degrees
NOISE PERFORMANCE						
Peak-to-Peak Noise	e_n p-p	0.1 Hz to 10 Hz		2.4		μV p-p
Voltage Noise Density	e_n	f = 1 kHz		10		nV/√Hz
		f = 10 kHz		8		nV/√Hz
Channel Separation	CS	f = 10 kHz		−115		dB

V_{DD} = 16 V, V_{CM} = V_{DD}/2, T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	V_{CM} = 8 V		0.6	2.5	mV
		V_{CM} = −0.1 V to +14.0 V			3.0	mV
		−40°C < T_A < +125°C			5.0	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C < T_A < +125°C		3.0	10	μV/°C
Input Bias Current	I_B			0.2	1	pA
		−40°C < T_A < +125°C			550	pA
Input Offset Current	I_{OS}			0.1	0.5	pA
		−40°C < T_A < +125°C			70	pA
Input Voltage Range	V_{CM}		−0.1		+14.0	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = −0.1 V to +14.0 V	90	110		dB
		−40°C < T_A < +125°C	80			dB
Large-Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, V_O = 0.5 V to 15.5 V	130	255		V/mV
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_{OUT} = 1 mA	15.94	15.96		V
		−40°C < T_A < +125°C	15.90			V
Output Voltage Low	V_{OL}	I_{OUT} = 1 mA		22	40	mV
		−40°C < T_A < +125°C			50	mV
Short-Circuit Output Current	I_{SC}			±140		mA
Closed-Loop Output Impedance	Z_{OUT}	At 1 MHz, A_V = 1		50		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{DD} = 5.0 V to 16 V	98	115		dB
		−40°C < T_A < +125°C	94			dB
Supply Current per Amplifier	I_{SY}			1.15	1.55	mA
		−40°C < T_A < +125°C			2.0	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ		3.5		V/μs
Gain Bandwidth Product	GBP			4		MHz
Phase Margin	Φ_M			73		Degrees
NOISE PERFORMANCE						
Peak-to-Peak Noise	e_n p-p	0.1 Hz to 10 Hz		2.5		μV p-p
Voltage Noise Density	e_n	f = 1 kHz		10		nV/√Hz
		f = 10 kHz		8		nV/√Hz
Channel Separation	CS	f = 10 kHz		−115		dB

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	18 V
Input Voltage	GND to V_{DD}
Differential Input Voltage	±18 V
Output Short-Circuit to GND	Indefinite
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +125°C
Lead Temperature (Soldering, 60 sec)	300°C
Junction Temperature	150°C

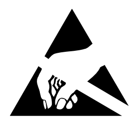
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
5-Lead SOT-23 (RJ-5)	240	92	°C/W
8-Lead SOIC_N (R-8)	158	43	°C/W
8-Lead MSOP (RM-8)	210	45	°C/W
14-Lead SOIC (R-14)	120	36	°C/W
14-Lead TSSOP (RU-14)	180	35	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

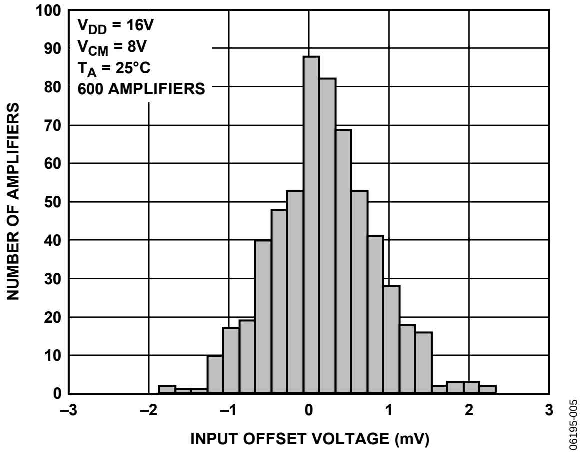


Figure 7. Input Offset Voltage Distribution

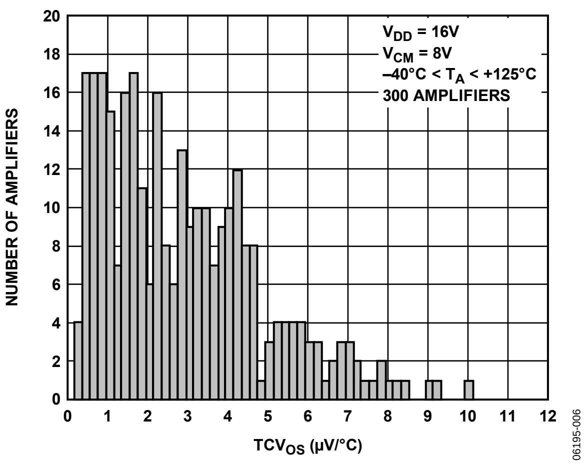


Figure 8. V_{OS} Drift (TCV_{OS}) Distribution

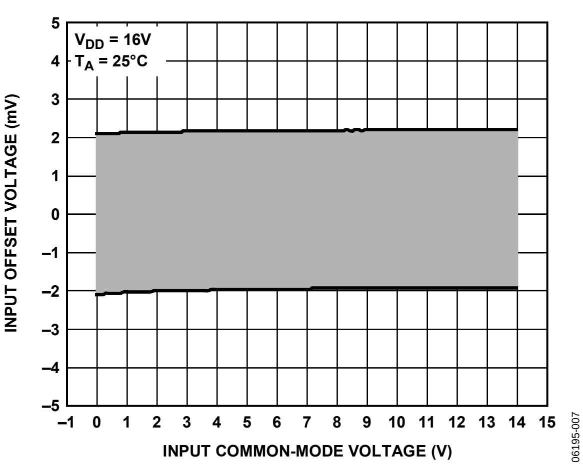


Figure 9. Offset Voltage vs. Common-Mode Voltage

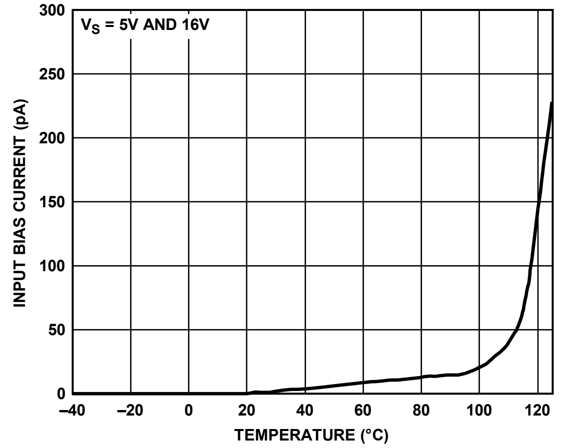


Figure 10. Input Bias Current vs. Temperature

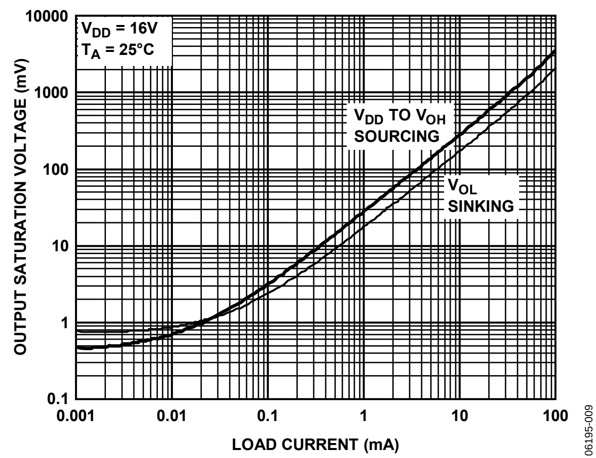


Figure 11. Output Saturation Voltage vs. Load Current

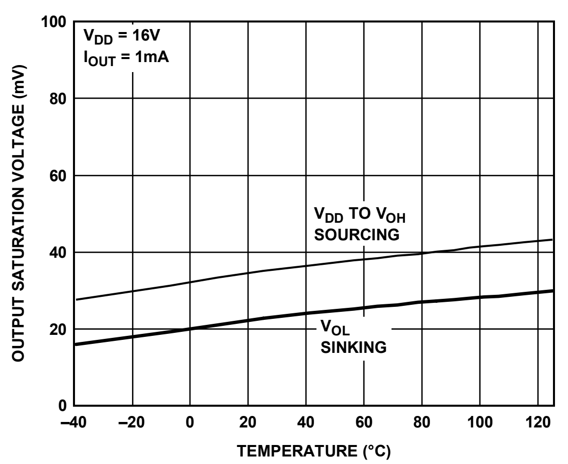


Figure 12. Output Saturation Voltage vs. Temperature

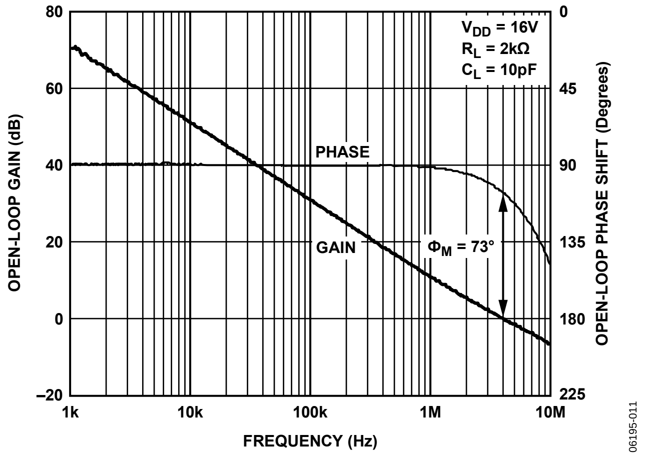


Figure 13. Open-Loop Gain and Phase vs. Frequency

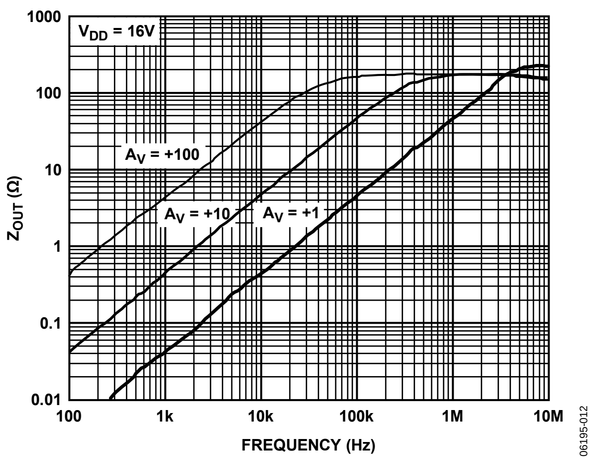


Figure 14. Closed-Loop Output Impedance vs. Frequency

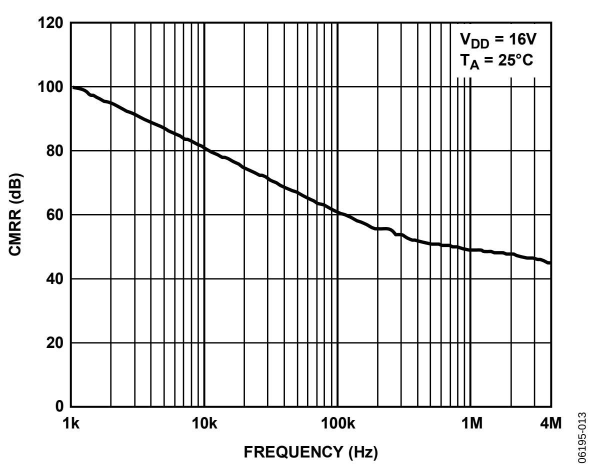


Figure 15. Common-Mode Rejection Ratio vs. Frequency

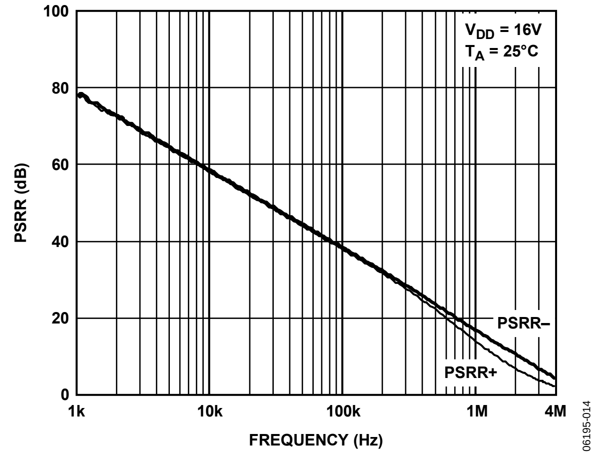
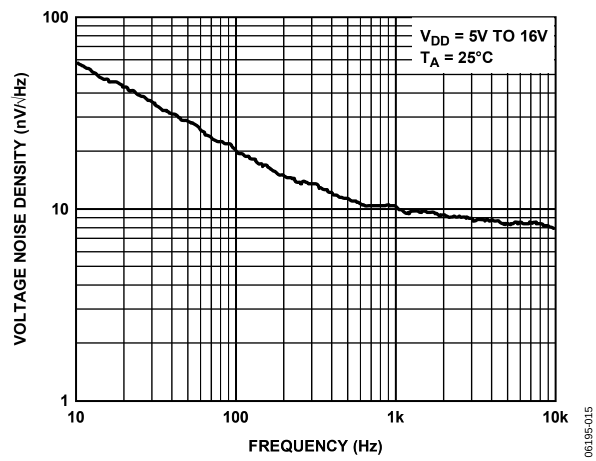


Figure 16. Power Supply Rejection Ratio vs. Frequency



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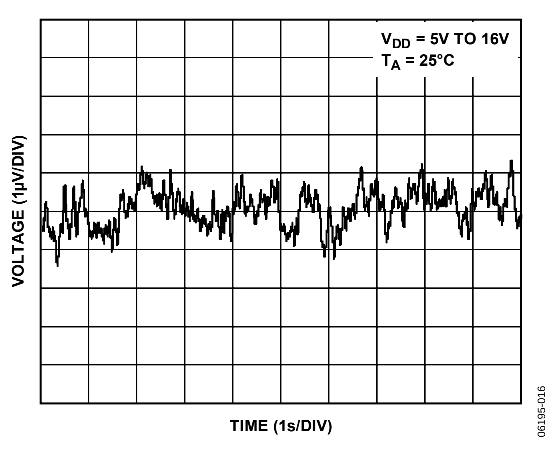


Figure 18. 0.1 Hz to 10 Hz Voltage Noise

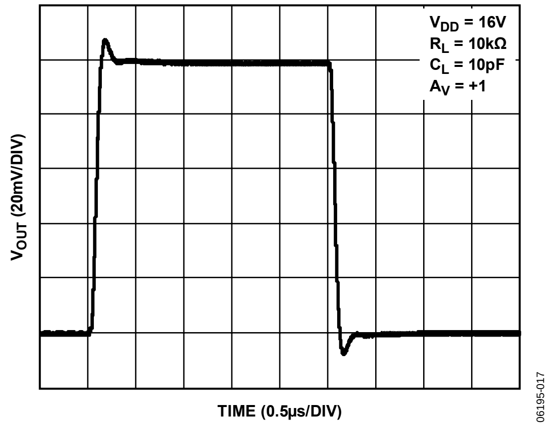


Figure 19. Small-Signal Transient Response

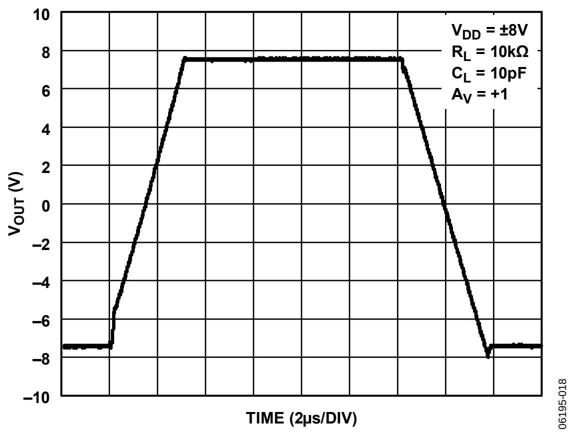


Figure 20. Large-Signal Transient Response

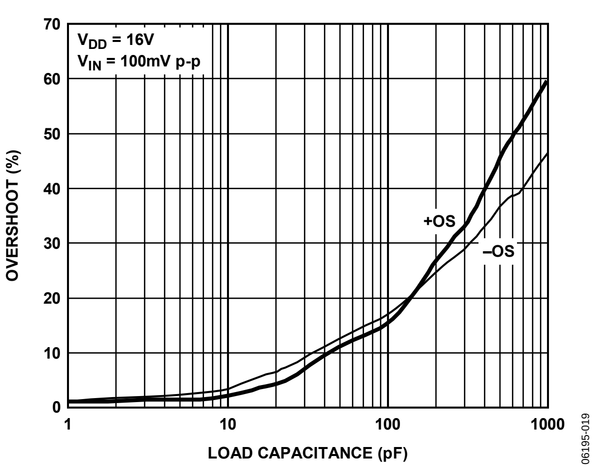


Figure 21. Small-Signal Overshoot vs. Load Capacitance

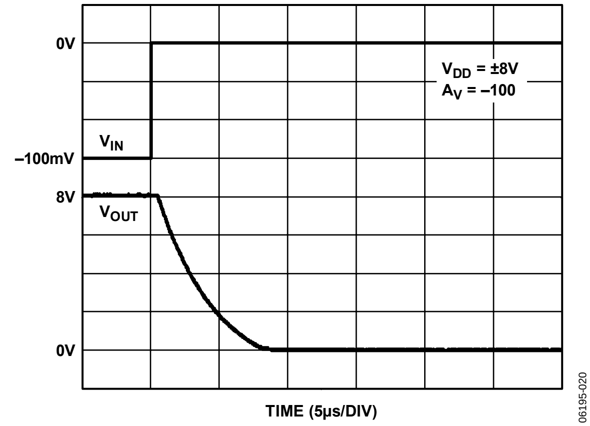


Figure 22. Positive Overload Recovery Time

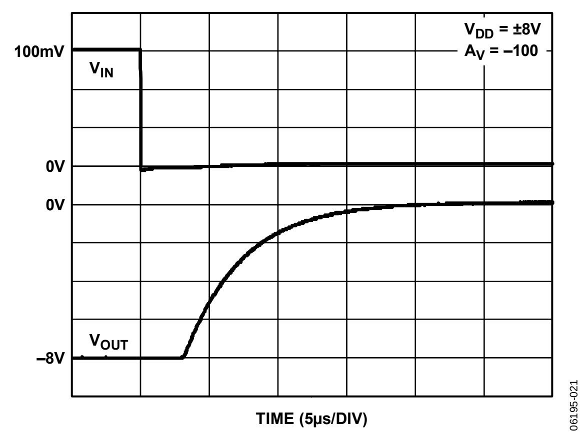


Figure 23. Negative Overload Recovery Time

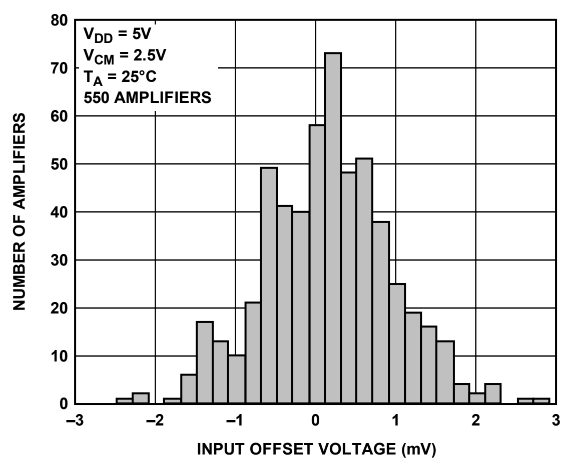


Figure 24. Input Offset Voltage Distribution

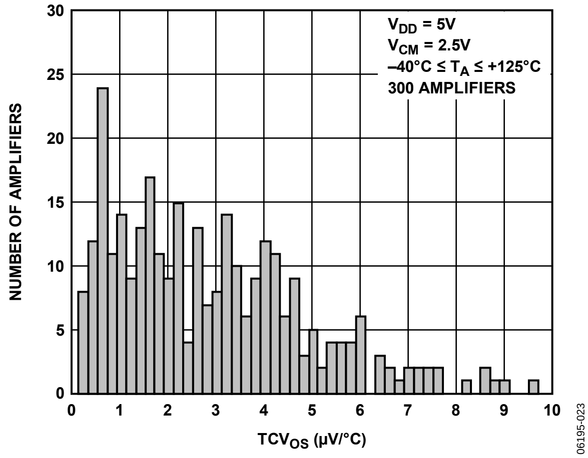


Figure 25. V_{OS} Drift (TCV_{OS}) Distribution

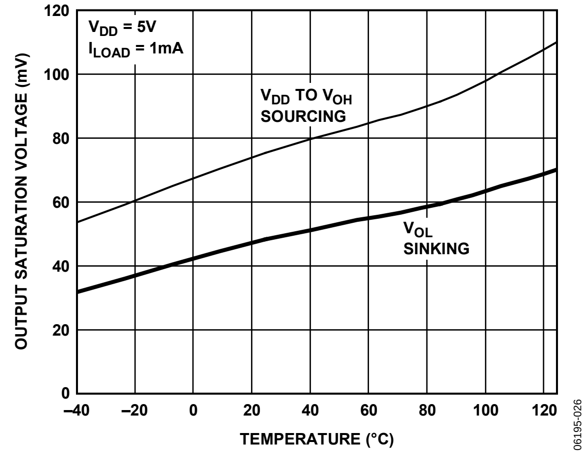


Figure 28. Output Saturation Voltage vs. Temperature

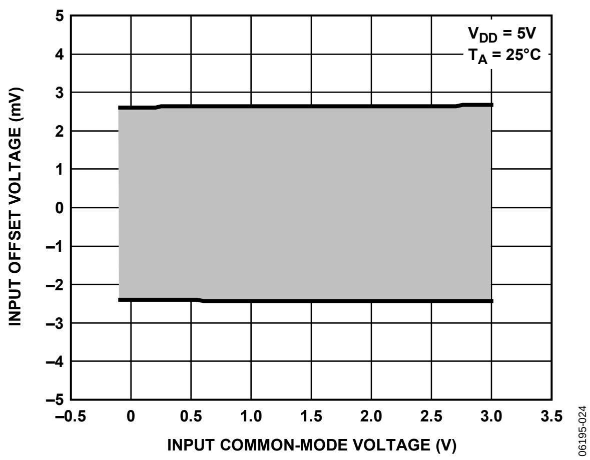


Figure 26. Offset Voltage vs. Common-Mode Voltage

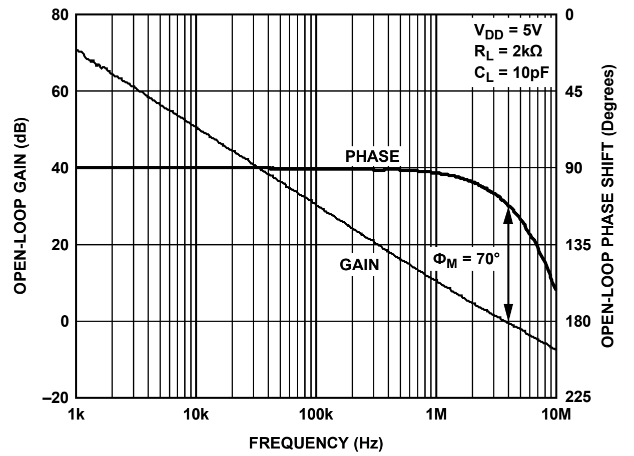


Figure 29. Open-Loop Gain and Phase vs. Frequency

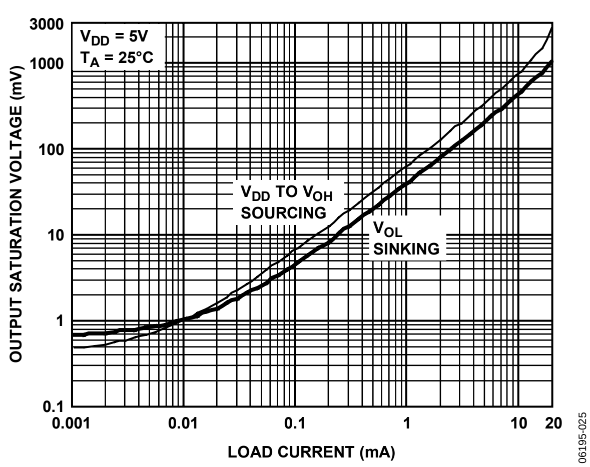


Figure 27. Output Saturation Voltage vs. Load Current

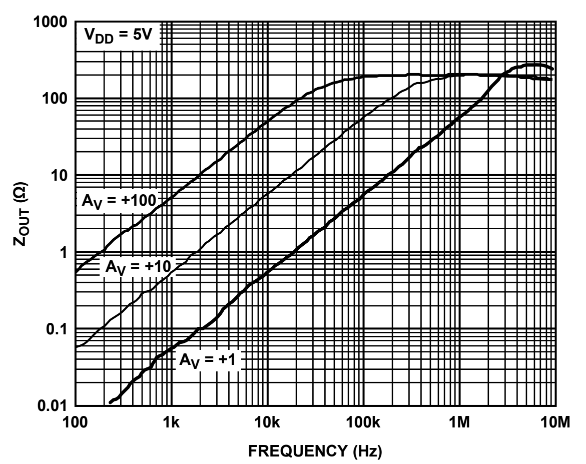


Figure 30. Closed-Loop Output Impedance vs. Frequency

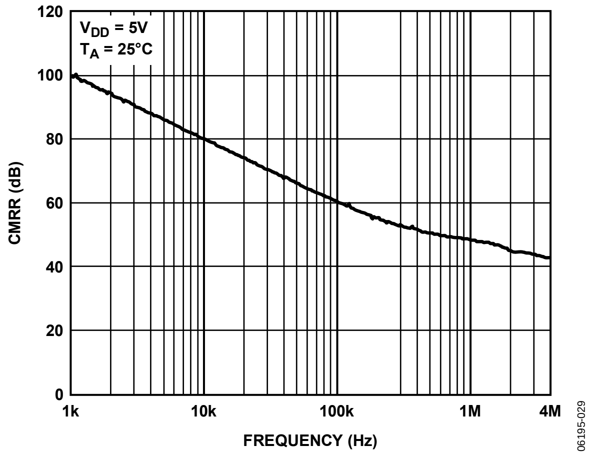


Figure 31. Common-Mode Rejection Ratio vs. Frequency

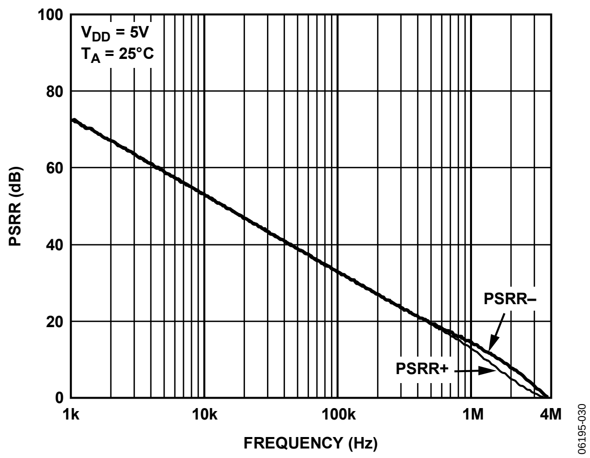


Figure 32. Power Supply Rejection Ratio vs. Frequency

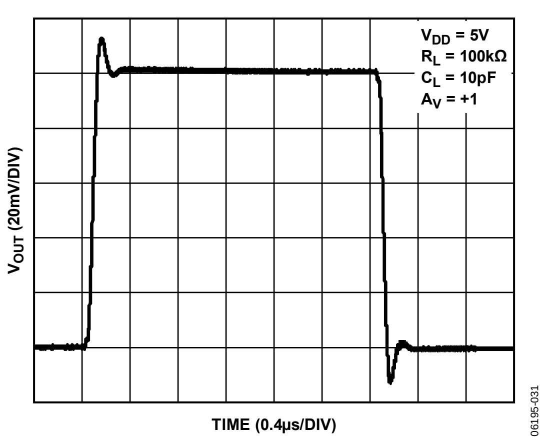


Figure 33. Small-Signal Transient Response

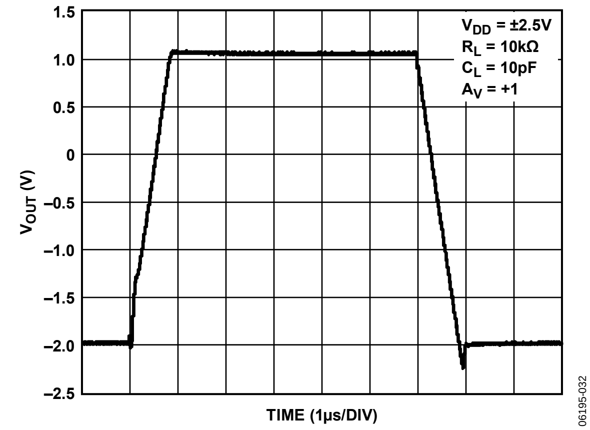


Figure 34. Large-Signal Transient Response

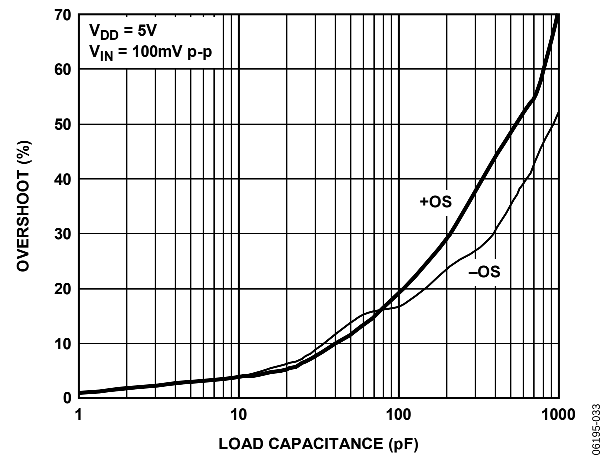


Figure 35. Small-Signal Overshoot vs. Load Capacitance

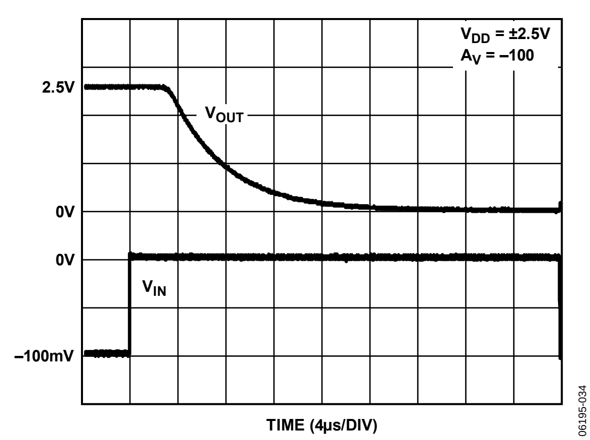


Figure 36. Positive Overload Recovery Time

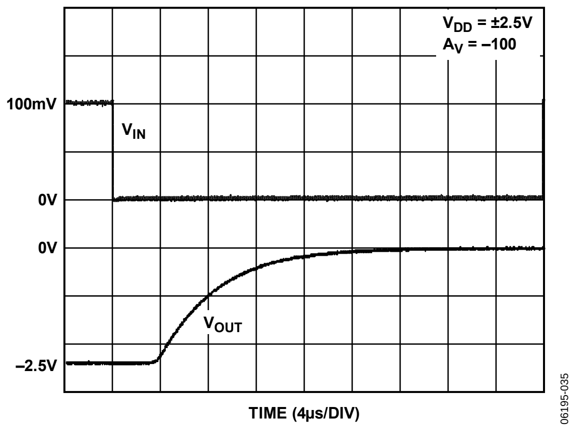


Figure 37. Negative Overload Recovery Time

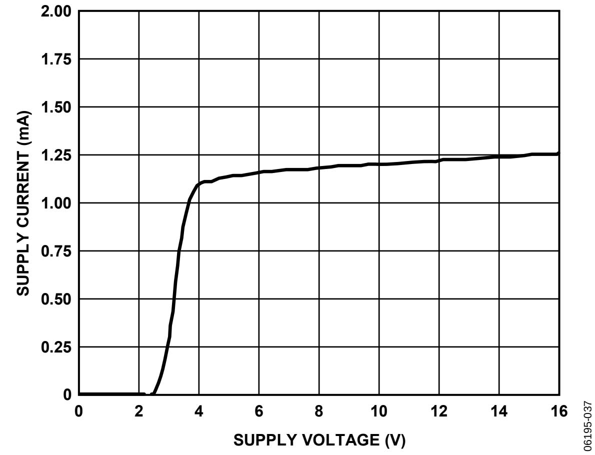


Figure 39. Supply Current vs. Supply Voltage

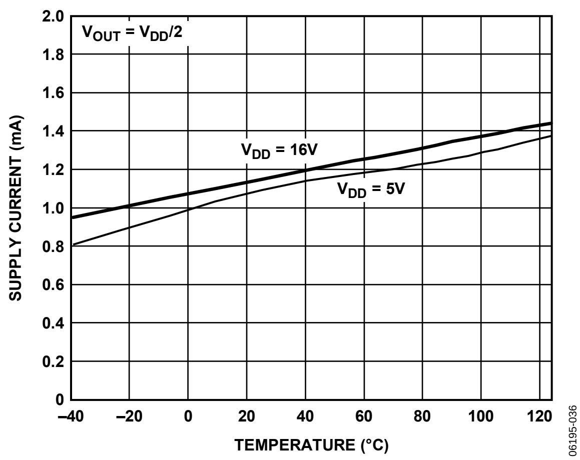


Figure 38. Supply Current vs. Temperature

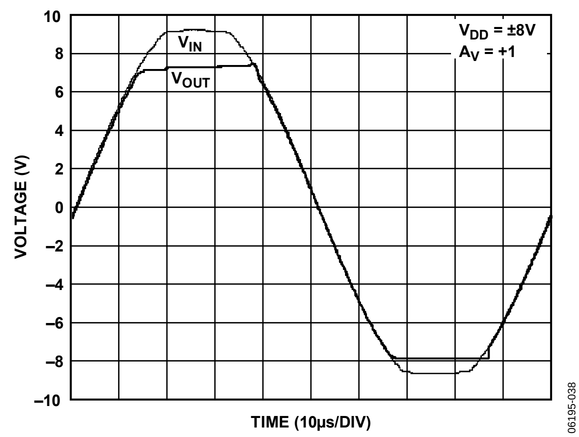
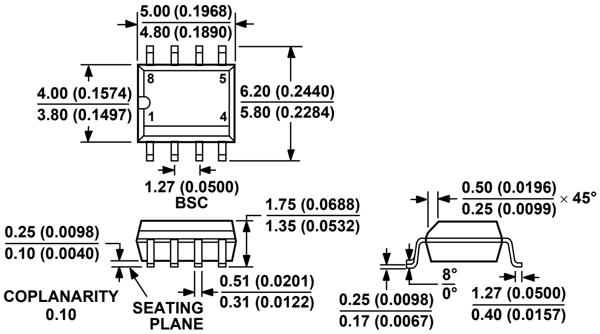


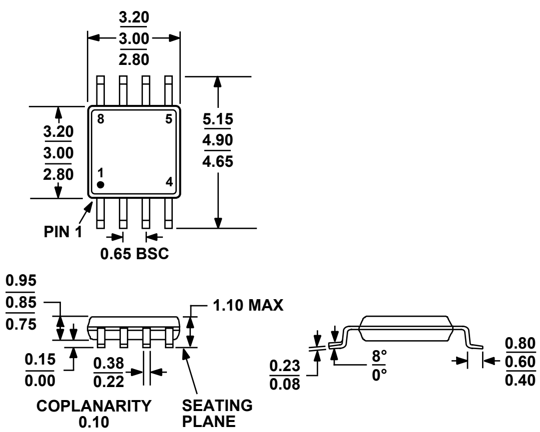
Figure 40. No Output Phase Reversal

OUTLINE DIMENSIONS



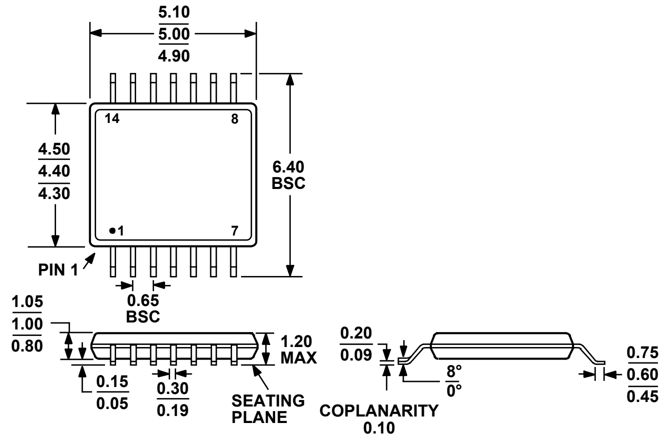
COMPLIANT TO JEDEC STANDARDS MS-012-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 41. 8-Lead Standard Small Outline Package [SOIC_N] Narrow Body (R-8) Dimensions shown in millimeters and (inches)



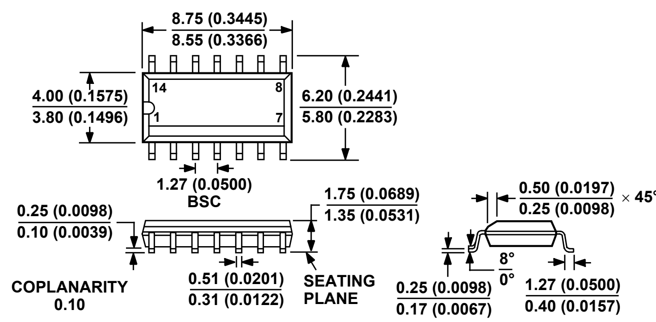
COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 42. 8-Lead Mini Small Outline Package [MSOP] (RM-8) Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-153-AB-1

Figure 43. 14-Lead Thin Shrink Small Outline Package [TSSOP] (RU-14) Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-012-AB
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 44. 14-Lead Standard Small Outline Package [SOIC_N] Narrow Body (R-14) Dimensions shown in millimeters and (inches)

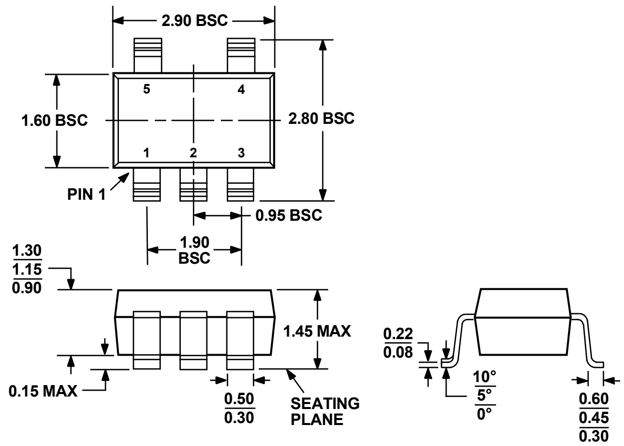


Figure 45. 5-Lead Small Outline Transistor Package [SOT-23]
(RJ-5)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
AD8665ARZ[1]	−40°C to +125°C	8-Lead SOIC_N	R-8	
AD8665ARZ-REEL[1]	−40°C to +125°C	8-Lead SOIC_N	R-8	
AD8665ARZ-REEL7[1]	−40°C to +125°C	8-Lead SOIC_N	R-8	
AD8665ARJZ-R2[1]	−40°C to +125°C	5-Lead SOT-23	RJ-5	A1B
AD8665ARJZ-REEL[1]	−40°C to +125°C	5-Lead SOT-23	RJ-5	A1B
AD8665ARJZ-REEL7[1]	−40°C to +125°C	5-Lead SOT-23	RJ-5	A1B
AD8666ARZ[1]	−40°C to +125°C	8-Lead SOIC_N	R-8	
AD8666ARZ-REEL[1]	−40°C to +125°C	8-Lead SOIC_N	R-8	
AD8666ARZ-REEL7[1]	−40°C to +125°C	8-Lead SOIC_N	R-8	
AD8666ARMZ-R2[1]	−40°C to +125°C	8-Lead MSOP	RM-8	A16
AD8666ARMZ-REEL[1]	−40°C to +125°C	8-Lead MSOP	RM-8	A16
AD8668ARZ[1]	−40°C to +125°C	14-Lead SOIC_N	R-14	
AD8668ARZ-REEL[1]	−40°C to +125°C	14-Lead SOIC_N	R-14	
AD8668ARZ-REEL7[1]	−40°C to +125°C	14-Lead SOIC_N	R-14	
AD8668ARUZ[1]	−40°C to +125°C	14-Lead TSSOP	RU-14	
AD8668ARUZ-REEL[1]	−40°C to +125°C	14-Lead TSSOP	RU-14	

[1] Z = Pb-free part.

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